CLAIMS

What is claimed is:

1. A method of forming a damascene interconnect structure in a semiconductor integrated circuit, the method comprising:

forming a trench in a first dielectric layer on a substrate;

forming a dielectric diffusion barrier film in the trench for preventing the diffusion of a copper interconnect metal layer into the first dielectric layer;

etching the dielectric diffusion barrier film anisotropically to remove the dielectric barrier film from the bottom surface of the trench to expose patterned metal;

depositing a barrier metal film in the trench to cover at least a portion of the bottom surface exposed by etching; and

filling the trench with a copper interconnect metal layer.

2. The method of forming a damascene interconnect structure in a semiconductor integrated circuit as recited in claim 1, further comprising forming a via aligned with the trench before forming a dielectric diffusion barrier film in the trench and wherein forming the dielectric diffusion barrier film in the trench is formed substantially simultaneously with the formation of the dielectric diffusion barrier film in the via.

3. The method of forming a damascene interconnect structure in a semiconductor integrated circuit as recited in claim 1, wherein the dielectric copper diffusion barrier layer is formed by one of CVD, PECVD, MOCVD, and ALD methods.

4. The method of forming a damascene interconnect structure in a semiconductor integrated circuit as recited in claim 1, wherein the barrier metal film further covers the sides of the trench.

5. The method of forming a damascene interconnect structure in a semiconductor integrated circuit as recited in claim 1, wherein the thickness of the barrier metal film formed on the sides of the trench is approximately 20 per cent or less of the thickness of the barrier metal film formed at the bottom of the trench.

6. The method of forming a damascene interconnect structure in a semiconductor integrated circuit as recited in claim 1, wherein the wherein the thickness of the barrier metal film formed on the sides of the trench is approximately 10 per cent or less of the thickness of the barrier metal film formed at the bottom of the trench.

7. The method of forming a damascene interconnect structure in a semiconductor integrated circuit as recited in claim 1, wherein the thickness of the barrier metal film formed on the bottom of the trench lies in the range of 10 to 100 Angstroms.

8. The method of forming a damascene interconnect structure in a semiconductor integrated circuit as recited in claim 1, wherein the thickness of the dielectric diffusion barrier film deposited lies in the range of 15 to 500 Angstroms.

9. The method of forming a damascene interconnect structure in a semiconductor integrated circuit as recited in claim 1, wherein the thickness of the dielectric diffusion barrier film lies in the range of 50 to 100 Angstroms.

10. The method of forming a damascene interconnect structure in a semiconductor integrated circuit as recited in claim 1, further comprising depositing a copper seed layer on the barrier metal layer prior to filling the trench with copper.

11. The method of forming a damascene interconnect structure in a semiconductor integrated circuit as recited in claim 10, wherein depositing a copper adhesion promoter occurs before depositing the copper seed layer.

12. The method of forming a damascene interconnect structure in a semiconductor integrated circuit as recited in claim 1, wherein the trench is continuously lined with at least one of the dielectric diffusion barrier film or metallic diffusion barrier layer.

13. The method of forming a damascene interconnect structure in a semiconductor integrated circuit as recited in claim 1, wherein the dielectric diffusion barrier film includes at least one of SiC, SiN, Boron Nitride, amorphous carbon, AlN and SiOC.

14. The method of forming a damascene interconnect structure in a semiconductor integrated circuit as recited in claim 1, wherein the dielectric diffusion barrier film is formed by surface treating the dielectric layer using high density plasma bombardment to direct Ar or H_2 particles to the dielectric layer.

15. The method of forming a damascene interconnect structure in a semiconductor integrated circuit as recited in claim 1, wherein the anisotropic etching of the diffusion barrier film is performed by a plasma etch.

16. The method of forming a damascene interconnect structure in a semiconductor integrated circuit as recited in claim 1, wherein the barrier metal deposition is controlled by a directional deposition of the barrier metal.

17. The method of forming a damascene interconnect structure in a semiconductor integrated circuit as recited in claim 16, wherein the directional deposition is performed using one of ionized metal plasma (IMP), high power self-ionized plasma (SIP), physical vapor deposition (PVD), and ionized physical vapor deposition (IPVD) methods.

18. A low resistance damascene interconnect structure comprising:

a trench formed in a dielectric layer on a substrate;

a dielectric diffusion barrier film formed on the sidewalls of the trench;

a metallic barrier film formed on the bottom of the trench, wherein at least one of the dielectric diffusion barrier film and a metallic barrier film are formed continuously over the inside surface of the trench and configured to prevent the diffusion of copper into either the first dielectric layer or a dielectric layer positioned below the trench; and

a planarized copper conductor filling the trench.

19. The low resistance damascene interconnect structure as recited in claim 18 wherein the dielectric diffusion barrier film includes at least one of SiC, SiN, Boron Nitride, amorphous carbon, AlN and SiOC.

20. A low resistance damascene interconnect structure as recited in claim 18 wherein the trench is part of a dual damascene structure.

21. A low resistance damascene interconnect structure as recited in claim 18 wherein the dielectric diffusion barrier film has a thickness of 15 to 500 Angstroms.

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